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| ART UNIT | PAPER NUMBER |
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| 3663 | |

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/751,714 | LUK ET AL. | |
| | Examiner | Art Unit | |
| | Johannes P. Mondt | 3663 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,9,10,13-15,21,23,31 and 35* is/are rejected.

7)☒ Claim(s) *3-8,11,12,16-20,22,24-30,32-34,36 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

Amendment filed 12/15/05 forms the basis for this office action. In said Amendment applicant cancelled claims 38-42, substituted replacement sheets for drawings 2B, 5B, 7 and 9, and responded in traverse to the rejections of claims 1, 2, 9, 10, 13-15, 21, 23, 31 and 35 made in the previous office action.

Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

### *Drawings*

In order to avoid abandonment, the drawing informalities noted in the paper mailed on 9/14/05, must now be corrected. Correction can only be effected in the manner set forth in the above noted paper.

1. *Figures 1B, 2B, 4B, 5B, 6, 7, 8 and 9* should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see page 8, lines 10-18). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheets should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not acceptable to the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(b) because they are incomplete. 37 CFR 1.83(b) reads as follows:

> When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the connection of the invention therewith.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

In particular, the Drawings do not show any electrical connection between the control line and the signal line, yet Applicant claims modifying the voltage on the control line, whereby the sensed voltage (necessarily the same as the voltage on the signal

line) will be amplified when a voltage on the first terminal relative to the second terminal is above threshold and not amplified when it is not (claim 22).

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. ***Claims 1-2, 9-10, 13-15, 21, 23, 31 and 35*** are rejected under 35 U.S.C. 102(b) as being anticipated by Mead et al (5,844,265).

*Mead et al teach* (title, abstract, Figures 1, 3, 6, 7, and 9; cols. 2-10) a circuit 10 (col. 2, l. 65) for amplifying signals (abstract, first sentence), the circuit comprising:

a control line (LOAD BIAS connected to a bias voltage source) (cf. col. 3, l. 10-20 and Fig. 7); and

a two terminal semiconductor device 62-1 (MOS transistor used as varactor with source and drain short-circuited: col. 3, l. 33-43; cf. Fig. 1, 9 included as 62-1, 62-2, in Fig. 7), having first and second terminals (loc.cit.), the first terminal (gate of gated diode 62-2) coupled to a signal line 194-1 (of sense amplifier 10), and the second terminal coupled to the control line (capacitively, through 16-1) (loc.cit.), wherein the two terminal semiconductor device is adapted to have a capacitance (gate-channel/source/drain capacitance) when a voltage on the first terminal relative to the second terminal is above a threshold

voltage and to have a lower capacitance when the voltage on the first terminal relative to the second terminal is less than the threshold voltage (because the MOS varactor = gated diode inherently has a variable capacitor, wherein the gate voltage can be raised to cause depletion, and even further to cause inversion of the channel),

wherein the control line is adapted to be coupled to a control signal (through the capacitive coupling to the aforementioned bias voltage source); and

wherein the signal line is adapted to be coupled to a signal (from the vertical scanner) and to be an output of the circuit (through 218) (col. 8, l. 44-col. 9, l. 64).

*On claim 2:* the two terminal semiconductor device by Mead et al comprises a gated diode 62-1 (also 32 in Fig. 1) (Fig. 7) having a well (N.B.: substrate is a p-well; col. 5, l. 1-5; Fig. 3) because it is implemented as p-type substrate 156 (Fig. 6 and col. 7, l. 65) in Fig. 6, which inherently is a (electrostatic potential) well for all majority charge carriers therein) and wherein the threshold voltage can inherently be modified by modifying a dopant level in said well of the gated diode because said dopant level determines the number of charge carriers (see, for instance, Wolf, ISBN 0-961672-5-3, pages 116-133).

*On claim 9:* the circuit further comprises an output circuit 206-1 / 216 (Fig.7) adapted to produce an output corresponding to a voltage at the gate input of the gated diode (depending as it is on the capacitance of capacitor 62-1).

*On claim 10:* the output circuit comprises one or more of the following: a buffer, an inverter, and a latch, because the hold/sample circuit 206 (col. 9, l. 25-32) is a buffer circuit.

*On claim 13:* the two terminal semiconductor device comprises a gated diode 32 (62-1, 62-2) (col. 3, l. 33-43) (N.B.: source and drain both connected to the output of the sense amplifier and hence also to each other, forming one pole of the diode, the gate forming the other one).

*On claims 14-15:* the gated diode is an n-type gated diode (col. 3, l. 36) or a p-type gated diode (col. 3, l. 33-35), wherein the threshold voltage is a positive, respectively negative voltage (inherently, a positive voltage is required to cause inversion in the former, a negative voltage in the latter, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal relative to the second terminal is more positive, respectively negative, than the threshold voltage and to have a lower capacitance when the voltage on the first terminal is less positive, respectively negative, than the threshold voltage.

*On claim 21: Mead et al teach a* method for amplifying signals (cf. title), the method comprising the steps of: determining that a voltage on a signal line 194-1 (Fig. 7) is to be amplified (any voltage on input line 194-1 meets the claim limitation); and modifying voltage on a control line (LOAD BIAS) (by biasing the LOAD BIAS) (Fig. 7), wherein the control line is coupled to a second terminal (gate of 62-1) of a two terminal semiconductor device 62-2 (Fig. 7), the two terminal semiconductor device having the second terminal and a first terminal, the first terminal (terminal connected to both source

and drain of MOSFET 62-1 (col. 3, l. 33-43) coupled to the signal line, the second terminal coupled to the control line (loc.cit.), wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal is above a threshold voltage and to have a lower capacitance when the voltage on the first terminal is less than the threshold voltage (such adaptation, given the selection of a MOSFET for said two-terminal device, with source and drain directly connected, is unnecessary but instead it is inherent, given the creation of an inversion layer for large enough voltage; it is also specifically cited as said device is a varactor, i.e., variable capacitor: see col. 3, l. 27-43)) and wherein the control line is adapted to be coupled to a control signal (LOAD BIAS; loc.cit.) and wherein the signal line is adapted to be coupled to a signal (through photo-sensor 184-1) and to be an output 218 of the circuit (col. 9, l. 54-64).

*On claim 23:* the two terminal semiconductor device comprises a gated diode (MOSFET with source and drain directly interconnected is a gated diode) (col. 3, l. 33-43) having a well (p-type substrate is an electrostatic well for charge carriers) (N.B.: substrate is a p-well; col. 5, l. 1-5; Fig. 3) and wherein, inherently, the threshold voltage can be modified by modifying a dopant level in the well of the gated diode: the more dopant available, the higher the charge in the capacitor can become).

*On claim 31:* the two-terminal device comprises a gated diode 62-1 (cf. Fig. 7 and col. 3, l. 33-43).

*On claim 35:* the method further comprises the step of determining an output corresponding to the signal (inherently so, because output inherently is looked at and hence determined).

***Allowable Subject Matter***

5. ***Claims 3-8, 11-12, 16-20, 22, 24-30, 32-34 and 36-37*** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Within the context of claims 1 and 21 the isolation device as claimed is not found in the prior art (claims 3-8 and 17-20 as dependent upon claim 1; and claims 24-28 and 36-37 as dependent upon claim 21); within the context of claims 1 and 21 the gated diode with overlapping source diffusion region and gate has not been found in the prior art (claims 11 and 12 as dependent upon claim 1 and claims 29 and 30 as dependent upon claim 29); within the context of claim 1 the differential signal circuit as recited in claim 16 has not been found; within the context of claim 21 the step involving amplification or not (that is: not at all) depending on whether said threshold voltage is exceeded as recited in claim 22 has not been found in the prior art; and within the context of claim 21 the further limitations of claims 32-34 have not been found in the prior art either: in this regard it is noted that Mead et al teach the n-gated diode when a positive signal is to be processed, in which case the voltage on the control line does not need to be modified to a positive voltage for reaching above-threshold voltage, the requirement instead being one of sufficient voltage difference between gate and source/drain voltage of the gated diode.

***Response to Arguments***

In response to Remarks with regard to the Drawings objection made in the previous action examiner wants to point out that Figure 2A merely represents the circuit

that is implied by the device of Prior Art Figure 2B and hence shares the same prior art status as Figure 2B. Similarly, Figure 5A merely represents the circuit implied by prior art Figure 5B and hence shares the same prior art status with Figure 5B. Furthermore, the specification clearly states that what is shown in Figures 1B, 4B, 6 and 8 are conventional (lines 10-18 of page 8 of the specification). Furthermore, par. [0010] of the specification clearly discusses gate diodes in the context of the background art, including gated diodes with (possibly only) one source/drain area, as pertains to the illustrations of Figures 1 and 4, 6 and 8. Therefore, the Drawing objection of said previous office action is being repeated for those drawings that have not been provided with the "Prior Art" label. Finally, on the issue of prior art, see Amin (4,999,812) on the definition of gated diode (col. 3, l. 17-55) as a PN junction underneath a gate, which is precisely Figures 1, 4, 6 and 8 in the specification. No additional NP junction is included in said definition.

With regard to the traverse of the objection to the specification, indirect support for the claimed invention is indeed found on pages 14-23, given the positive threshold for inversion layer formation. Said objection has been withdrawn.

With regard to applicant's comments in traverse of the art rejection over Mead, as a preliminary point the use of varactors do not have any patentable weight in claims 1-2, 9-10 and 13-15, because their use constitutes functional language: In reference to the claim language including limitations referring to intended use and other types of functional language, the limitations must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed

invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). Furthermore, that varactor structure "allows compression of the output signal over a wide dynamic range of input signals" in no way reflects on the inherent property of a three terminal MOS device with source and drain connected to be a device with two rather than three terminals. No other terminal is shown other than the terminal for the gate and the terminal for the common source/drain terminal (see also the Figure 7 in Mead cited by applicant). See also Amin (4,999,812) citing the definition of a gate diode as a PN junction under a gate (col. 3, l. 17-55)); parenthetically, an illustration of this definition immediately renders Figure 1 in applicant's specification other than isolation structures already admitted elsewhere to be found in the prior art (see Figures 2 and 5, for instance). Applicant is not specific on the alleged "at least a number of other limitations" Mead does not teach (page 15 of Remarks). Yet, with regard to the first allegation in the negative ("transistors 62-n in Fig. 7 are not directly connected..." the important point is that the voltage at the lower terminal of 62-n in Figure 7 is clearly influenced by the gate voltage on 16-2, which is the LOAB BIAS. Therefore, the varactors are indeed coupled to said LOAD BIAS, while since the gate voltage on 16-n is determined by said LOAD BIAS control line is an appropriate terminology for said LOAD BIAS. That the LOAD BIAS is a DC voltage does not impact at all on the forgoing argument, because its amplitude can be adjusted at any time. The cited portion of col.

3, l. 23-25 merely states the obvious, namely that a varactor may be connected between input and output of an amplifier", as represented by the figures. So may indeed be the CASCODE BIAS. Clearly, amplification must occur between input and output. Applicant fails to convince that said cited portion in Mead means that this interposition of the varactor of Mead disqualifies the LOAD BIAS to be a control line. Traverse of dependent claims appears to solely depend on the traverse of the rejection of the independent claims.

## *Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
February 25, 2006

JACK KEITH
SUPERVISORY PATENT EXAMINER